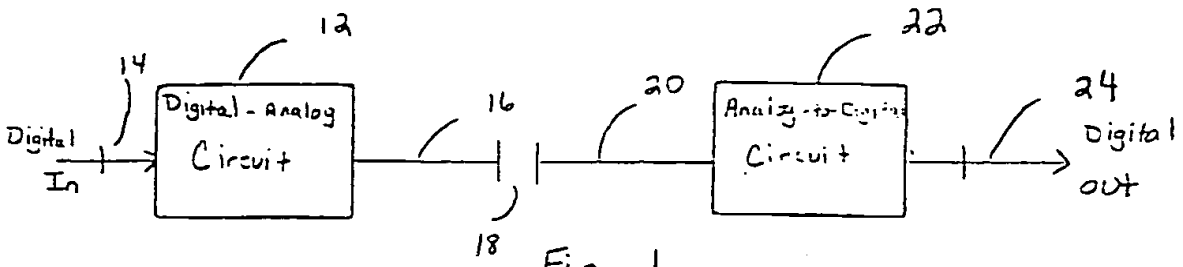


Fig. 1

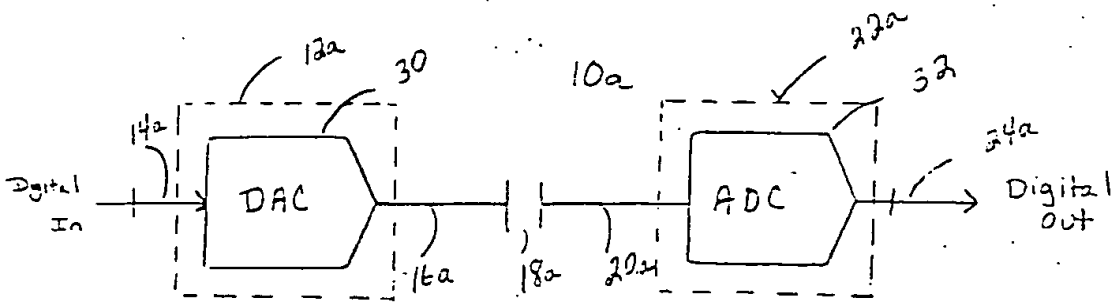


Fig. 2

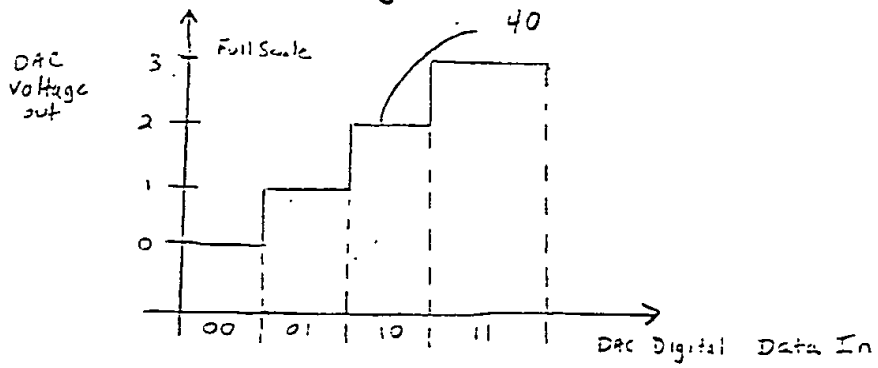


Fig. 3

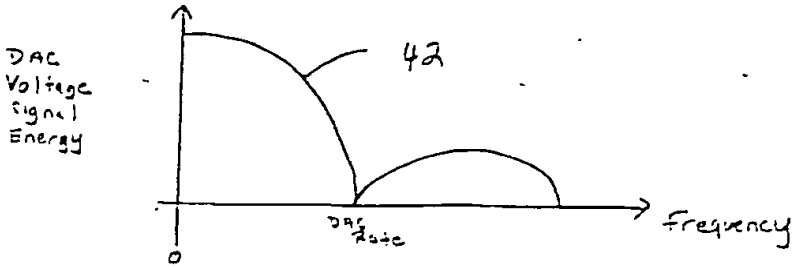


Fig. 4

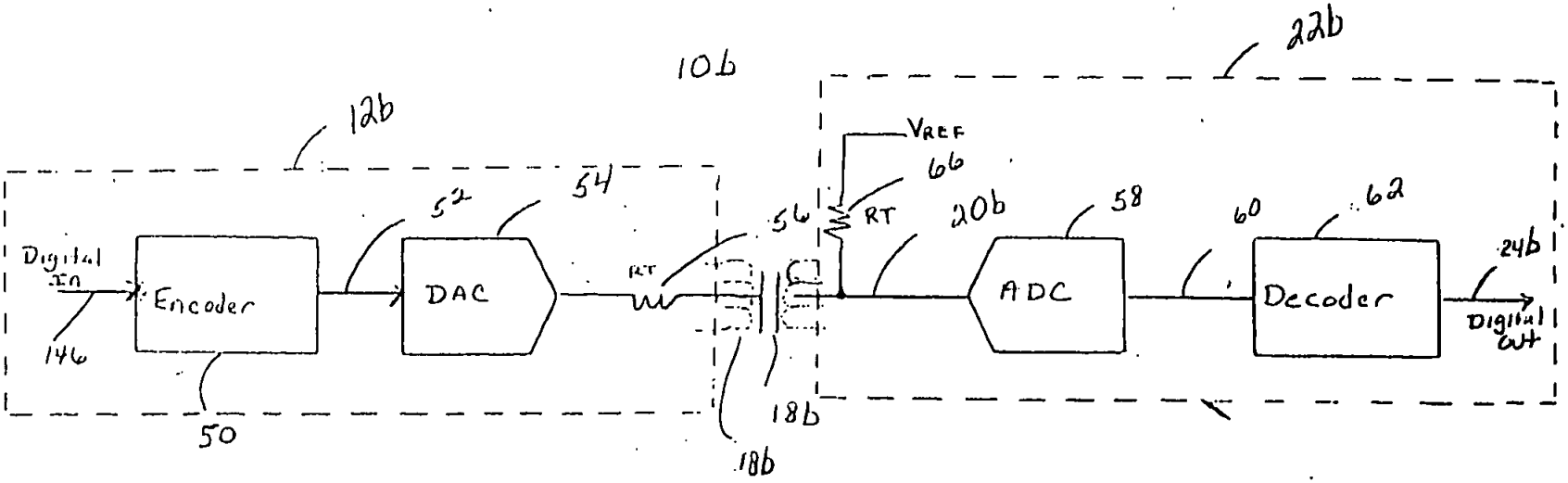

10b
12b
22b
Digital In
146
Encoder
50
52
DAC
54
RT
56
18b
18b
VREF
66
RT
20b
58
ADC
60
62
Decoder
24b
Digital out

Fig. 5

ENCODER

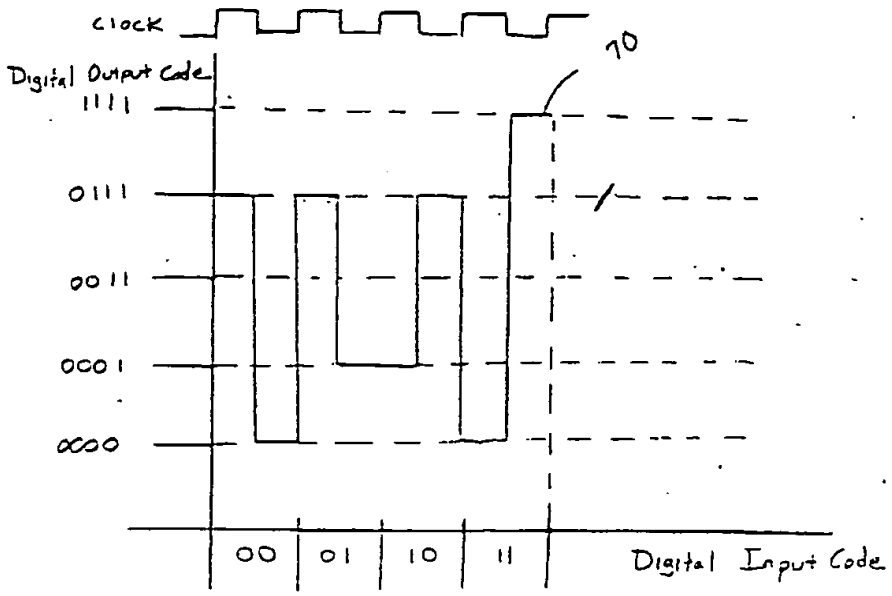


Fig. 6

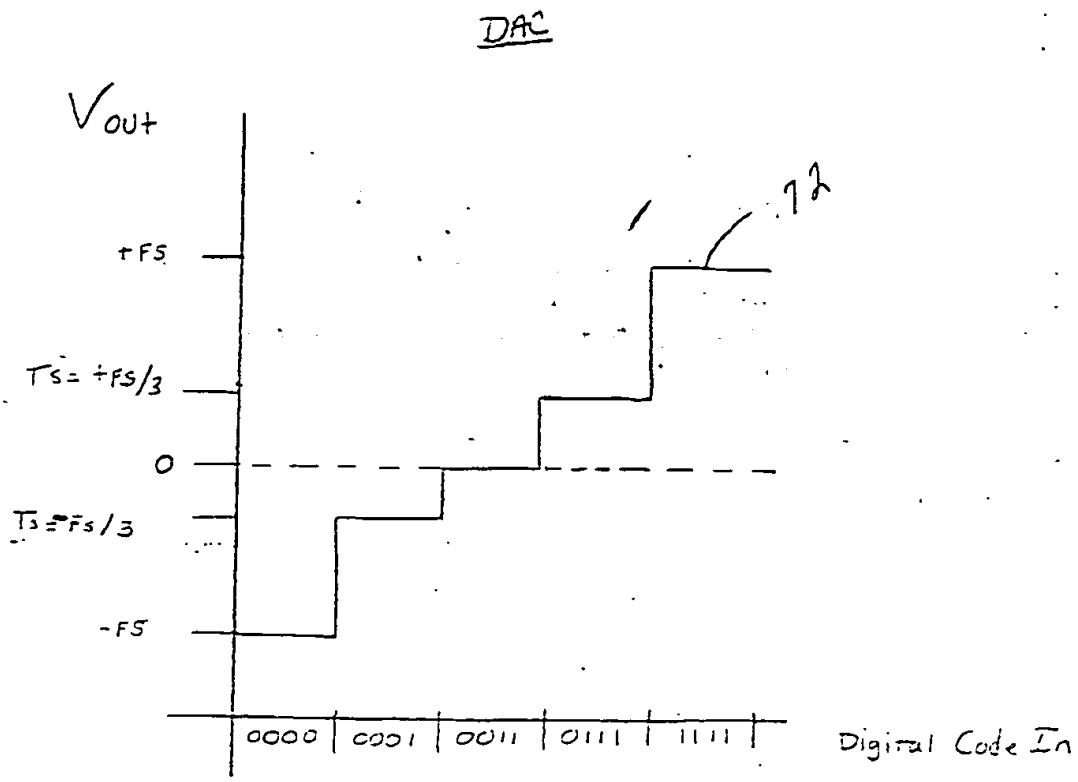
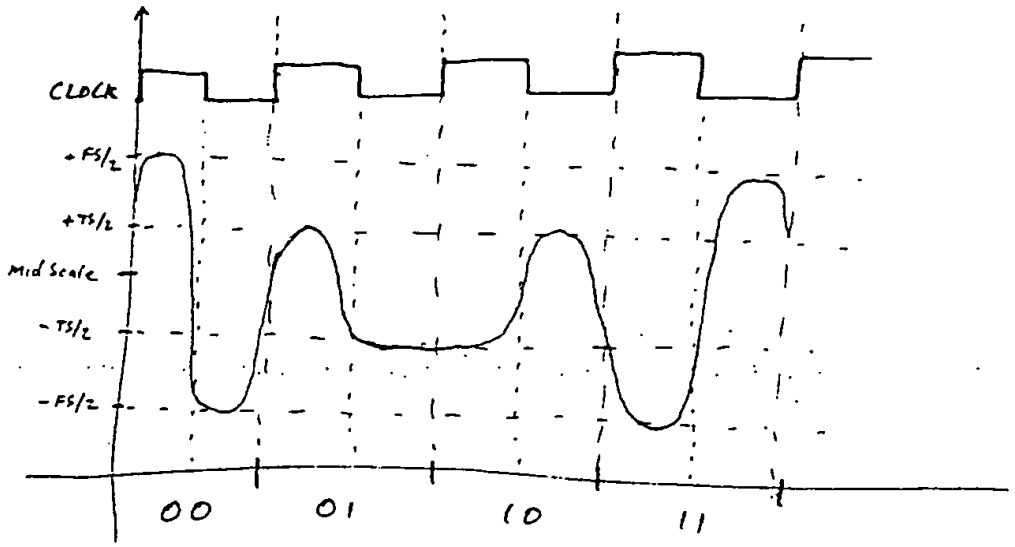

DAC
V_{OUT}
+FS
Ts = +FS/3
0
Ts = -Fs/3
-FS
0000
0001
0011
0111
1111
Digital Code In

Fig. 7

Fig. 8A Barrier Pin Signal



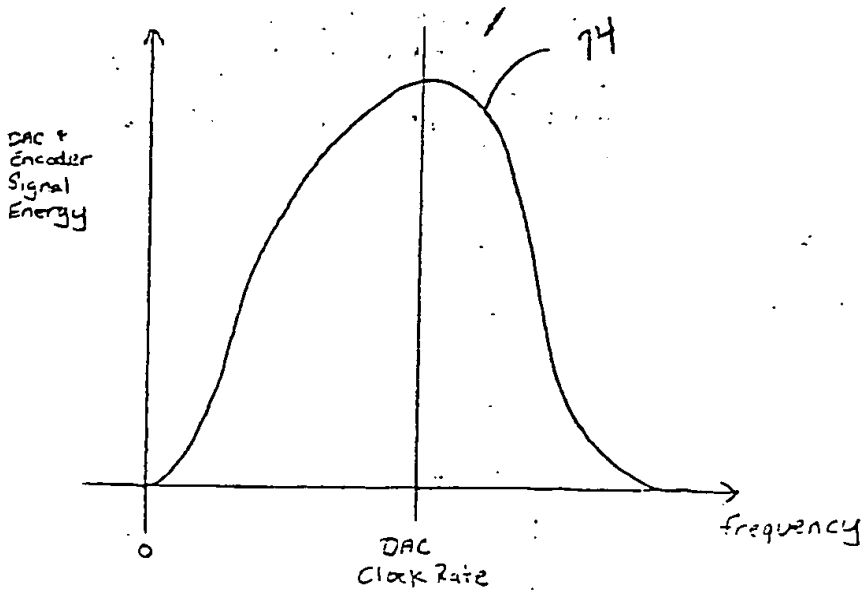
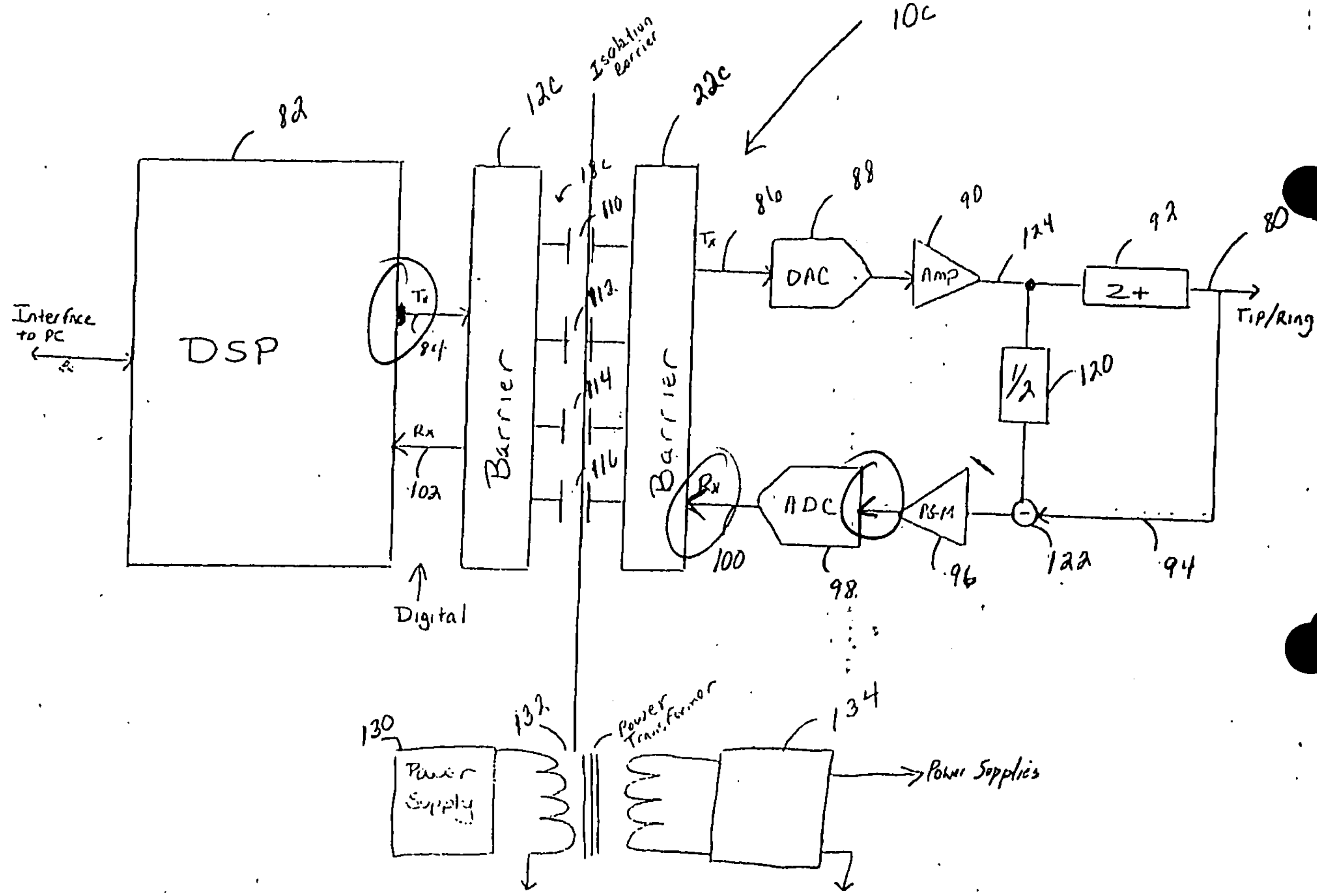
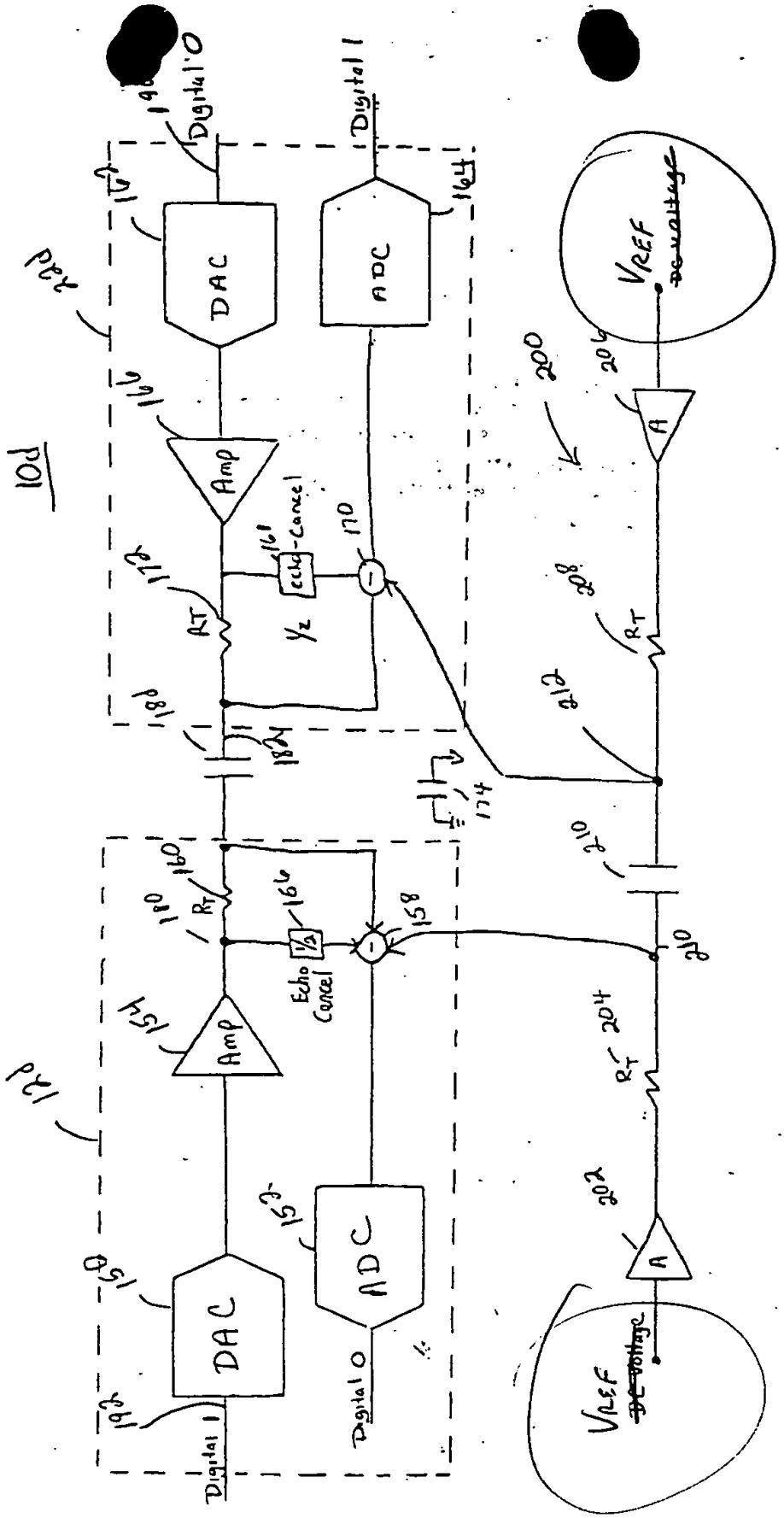


Fig. 8B



10c
82
DSP
Interface to PC
Tx
84
Rx
102
Digital
12c
Barrier
Isolation Barrier
18c
110
112
114
116
22c
Barrier
Tx
86
88
DAC
90
Amp
124
92
Z+
80
Tip/Ring
1/2
120
Rx
100
ADC
98
PGM
96
122
94
130
Power Supply
132
Power Transformer
134
Power Supplies

Fig. 9


Digital 0
Digital 1
DAC
ADC
Amp
Echo Cancel
½
RT
VREF
DC voltage
A
100
101
102
104
106
108
110
112
114
116
118
120
122
124
126
128
130
132
134
136
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210
212

Fig. 10

Full Barrier System

10e

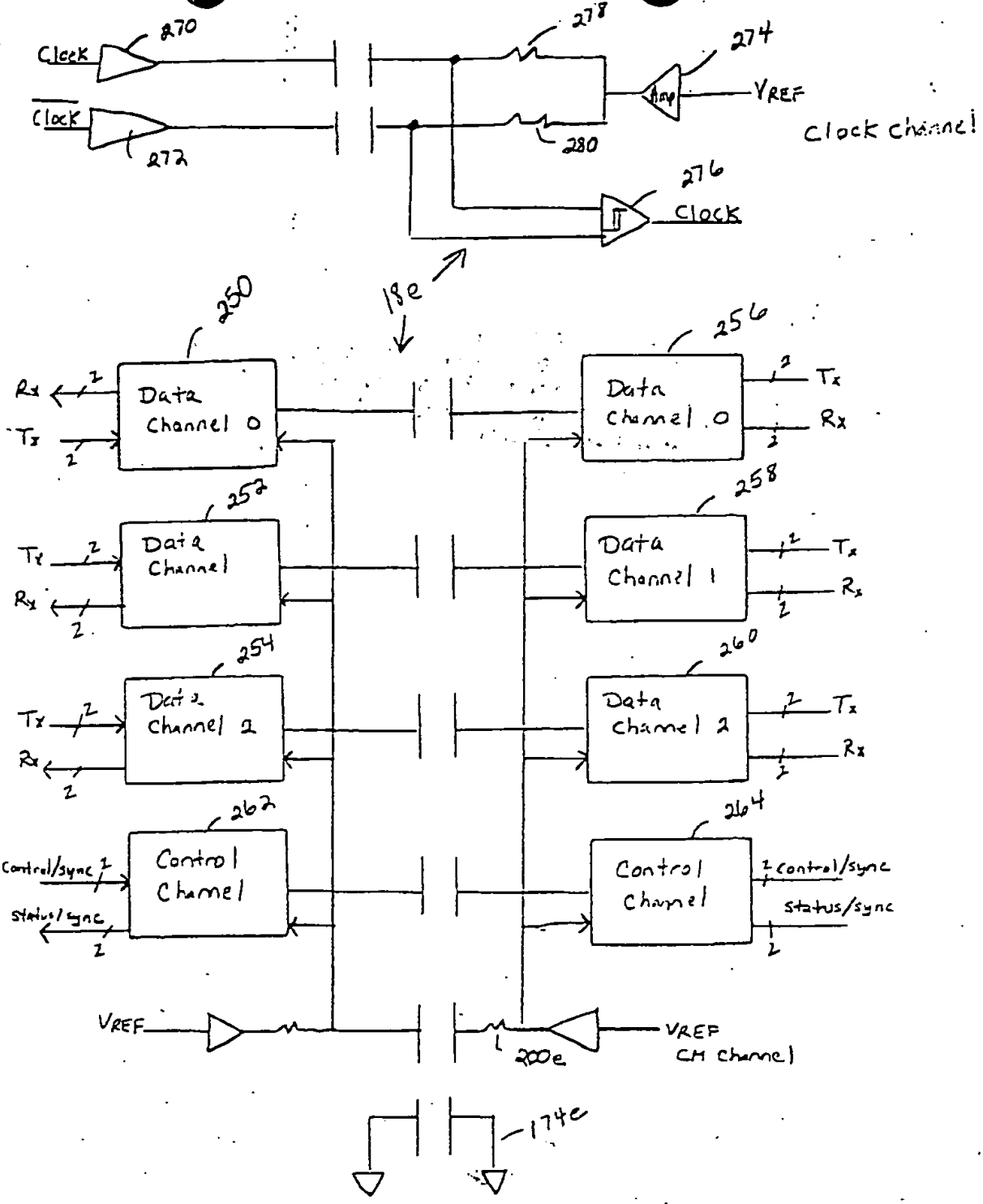

Fig. 11

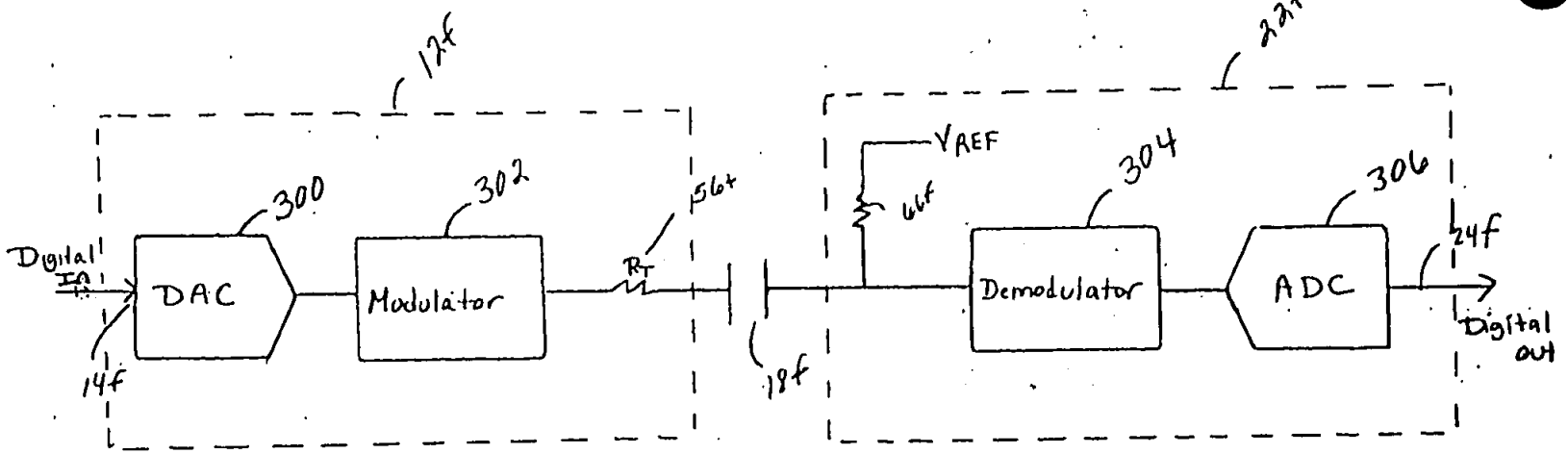

Fig. 12